REMARKS

By this amendment, Applicants have cancelled claims 5-7 and submitted corrected drawing Figures 1, 3, 4, 6 - 9, and 11.

The Examiner has rejected claims 5-6 under 35 U.S.C. 102(e) as being anticipated by Young et al. (U.S. Patent No. 6,775,342).

With respect to claim 5, Young et al. discloses, in Figs. 11 and 13; col. 19, lines 59-61 and col. 16, lines a circuit and its corresponding jitter inducing method comprising the steps of a) setting delay times for rising and/or falling edges of pulses in a reference pulse train [ref_clk] for sequential interval of the reference pulse train wherein changes to the delay times [1304] over the sequential intervals are controlled to be a desired function determined by parameters designated through a user interface [*col. 19, lines 59-61; note that delay line 1304 is indentical* to delay line 710_3], and b) providing pulses of the reference pulse train [234] in order of the corresponding intervals wherein delays are applied to the rising ans/or falling edges of the pulses by said delay time being set every interval.

With respect to claim 6, Young et al. discloses, in Figs. 11 and 13, that the changes of the delay time over the intervals are a function of a delayed time transition waveform [216/218].

The Examiner has rejected claim 7 under 35 U.S.C. 102(b) as being anticipated by Kim (U.S. Patent No. 5,880,612).

With respect to claim 7, Kin discloses, in Fig. 2, a circuit and its corresponding pulse generating method for providing a pulse train derived from a reference pulse train [234] divided into sequential intervals wherein delay times [232] applied to rising and/or falling edges of pulses in the reference pulse train are set interval by interval, and the changes of the delay times over the sequential intervals are controlled to be a desired function.

The Examiner has allowed claims 1-4 and 9-12.

The following statement of reasons for the indication of allowable subject matter:

The closest prior are of record does not show or fairly suggest:

a) A jitter inducing circuit including a switch control means for controlling a switch means to provide pulses to one delay means in which a setup of a delay time has finished, as called for in claim 1;

b) A jitter inducing method including steps of switching the supply of a reference pulse train to a second delay block from a first delay block and delaying the reference pulse train by the second delay block and providing an output to an output terminal, as called for in claim 9;

c) A circuit for generating a pulse train, in which a pulse providing means for providing a pulse to be jittered and a pulse not to be jittered to separate delay blocks of a plurality of delay blocks wherein both pulses are derived from a reference pulse train, and

the delay times for the delay block to which the non-jittered pulse is provided is fixed, and the delay time of the delay block to which the pulse to be jittered is provided changes sequentially, as called for in claim 11; and

d) A pulse generating method including the steps of (a) delaying rising edge or falling edge of a pulse to be jittered according to a preset delay time and (b) composing a non-jittered pulse and the pulse delayed in step (a) as called for in claim 12.

Applicants' arguments with respect to claim 5 has been considered but are moot in view of the new ground(s) of rejection.

Applicants' amendment necessitated the new ground(s) of rejection presented in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL.**

The Applicants hereby submit replacement sheets and annotated marked-up drawings of Figures 1, 3, 4, 6 - 9, and 11. Figures 1, 3, 4, 6 and 11 are corrected to remove unintentional artifacts in the drawings. Clams 7-9 are corrected to re-label elements to correspond more closely to the specification. The changes made to the drawing are outlined in red in the annotated marked-up drawings.

Applicants have cancelled claims 5-7 in the instant application. Claims 1-4 and 9-12 are deemed allowable by the Examiner.

In view of the cancellation of claims 5-7, Applicants respectfully request the Examiner pass this case to issue.

In accordance with current Patent Office practice, the Examiner is expressly authorized to call the undersigned agent at the number listed below if it is deemed the application is in other than condition for allowance or if prosecution can be expedited.

Respectfully submitted,

By _____
William K. Bucher
Reg. No. 32,686
Patent Agent for Applicants

TEKTRONIX, INC.
P. O. Box 500 (50-LAW)
Beaverton, OR 97077-0001
Phone (503) 627-7267 or (800) 835-9433
Attorney Docket No. 7465-US1

October 14, 2005

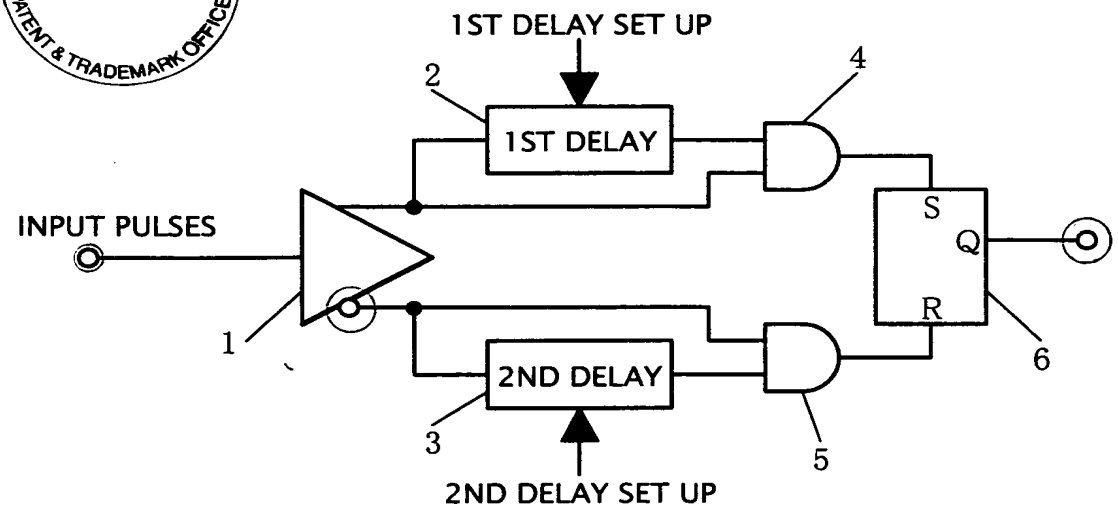

FIG. 1 (PRIOR ART)

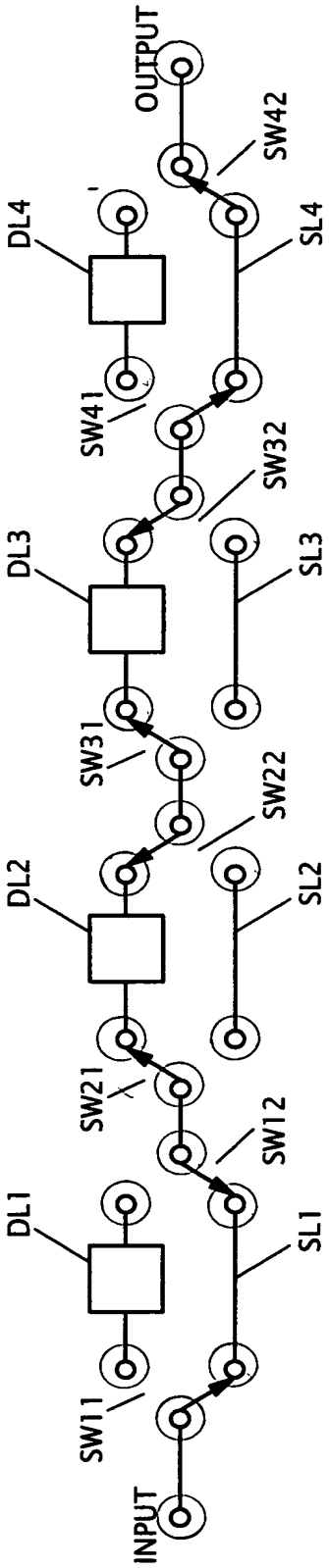

FIG. 3 (PRIOR ART)

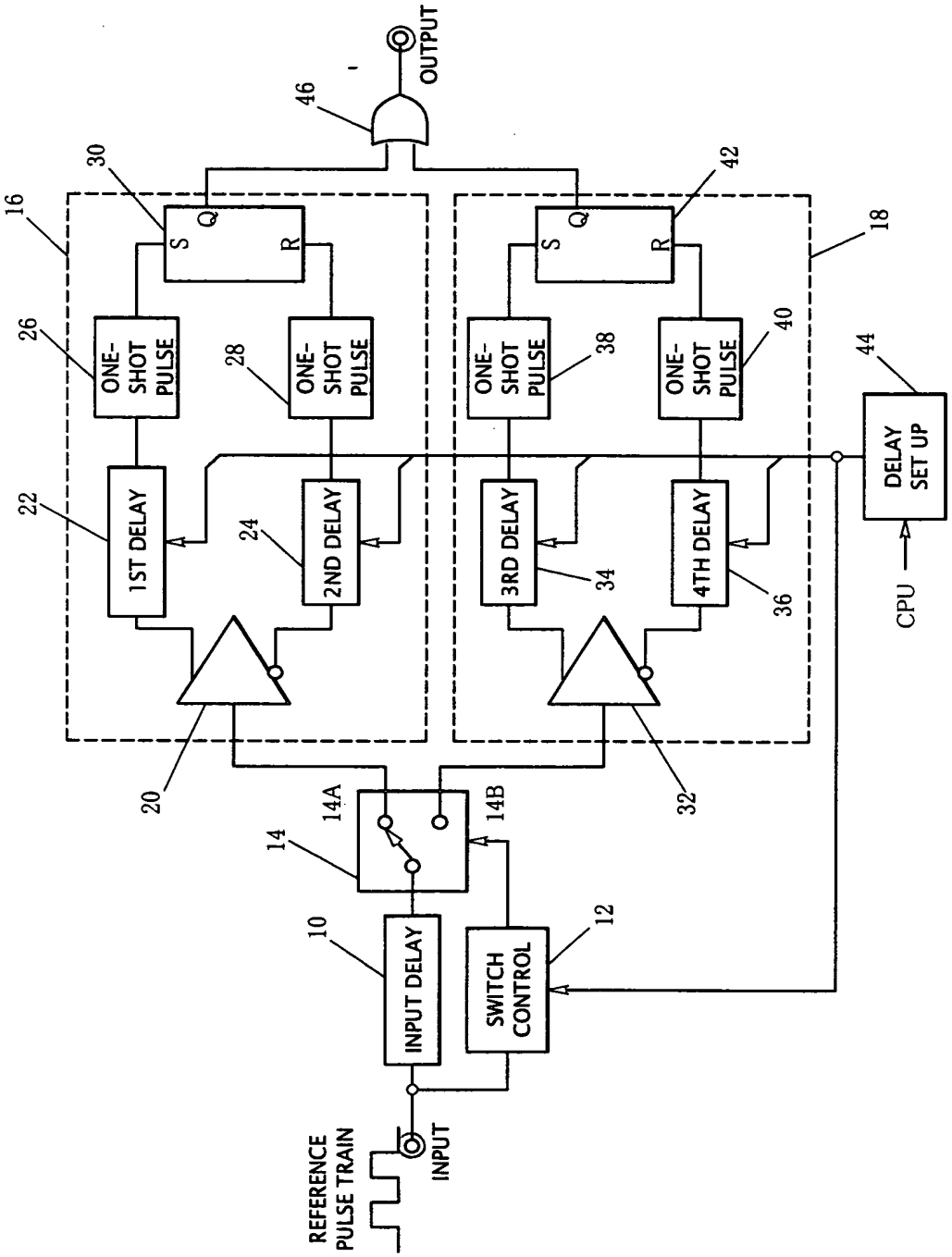
OUTPUT
46
30
42
16
18
S
Q
R
S
Q
R
26
ONE-SHOT PULSE
28
ONE-SHOT PULSE
ONE-SHOT PULSE
38
ONE-SHOT PULSE
40
44
DELAY SET UP
22
1ST DELAY
24
2ND DELAY
3RD DELAY
34
4TH DELAY
36
CPU
20
32
14A
14B
14
10
INPUT DELAY
SWITCH CONTROL
12
REFERENCE PULSE TRAIN
INPUT

FIG. 4

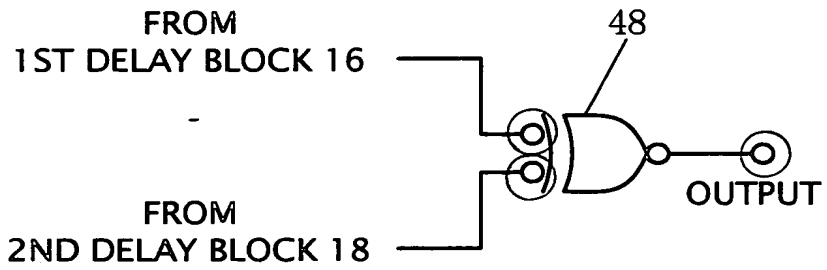

FIG. 6

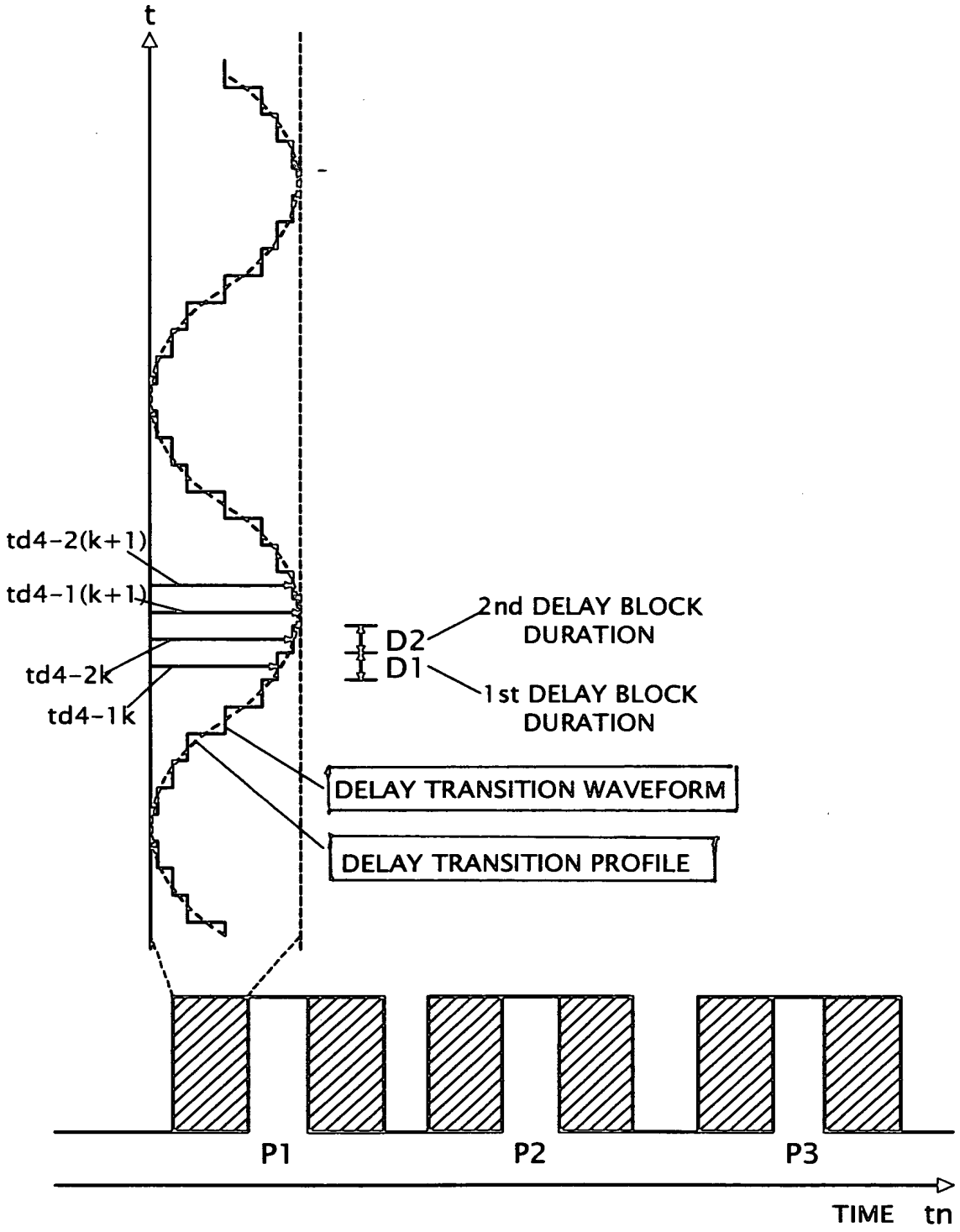
t
td4-2(k+1)
td4-1(k+1)
td4-2k
td4-1k
D2
D1
2nd DELAY BLOCK DURATION
1st DELAY BLOCK DURATION
DELAY TRANSITION WAVEFORM
DELAY TRANSITION PROFILE
P1
P2
P3
TIME tn

FIG. 7

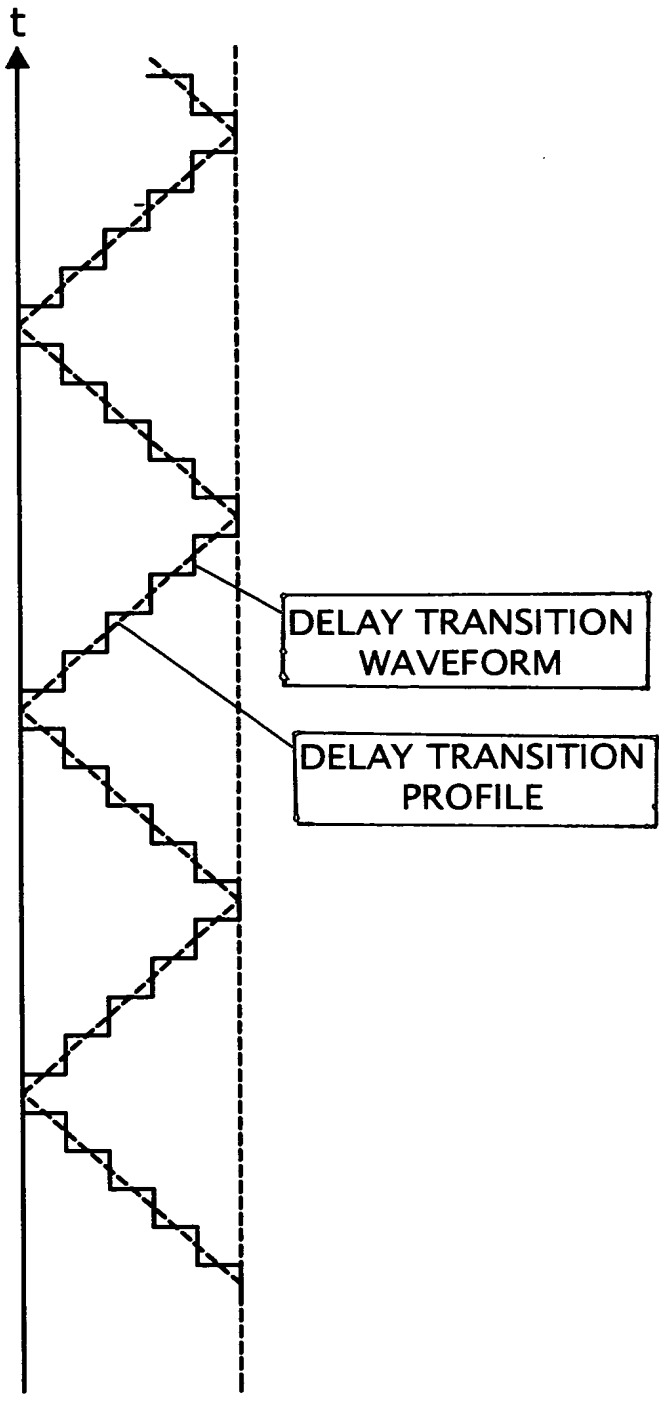

FIG. 8

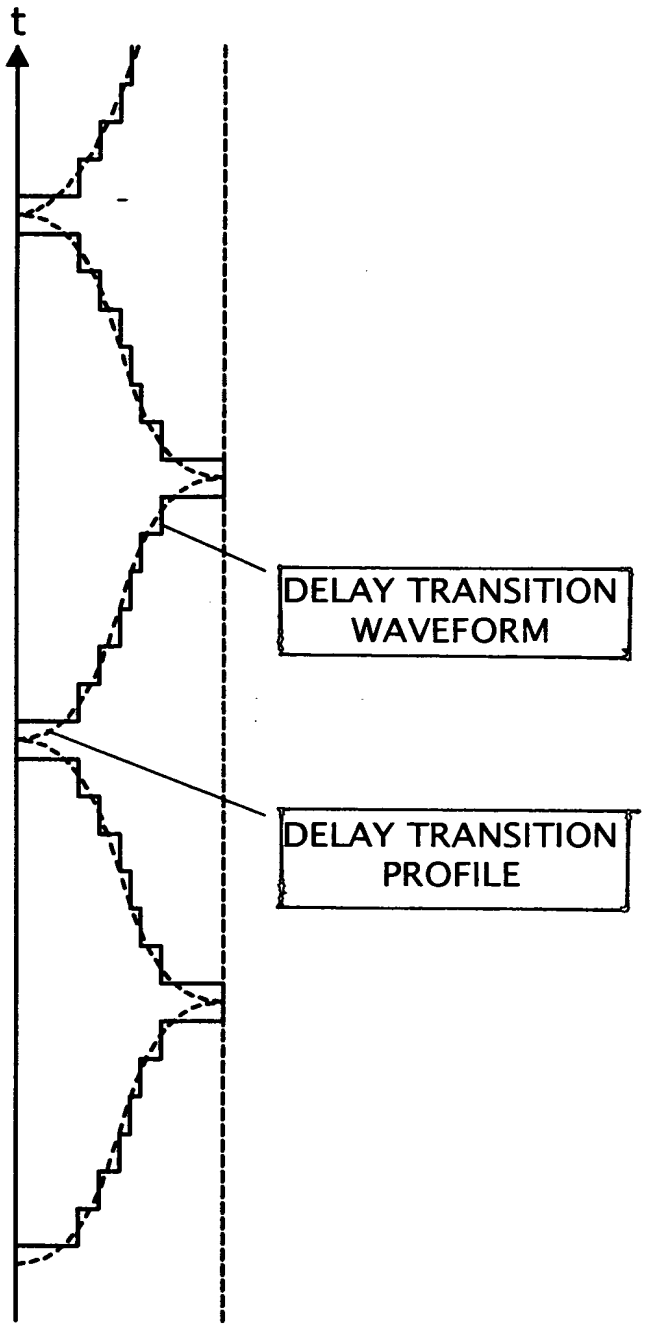

FIG. 9

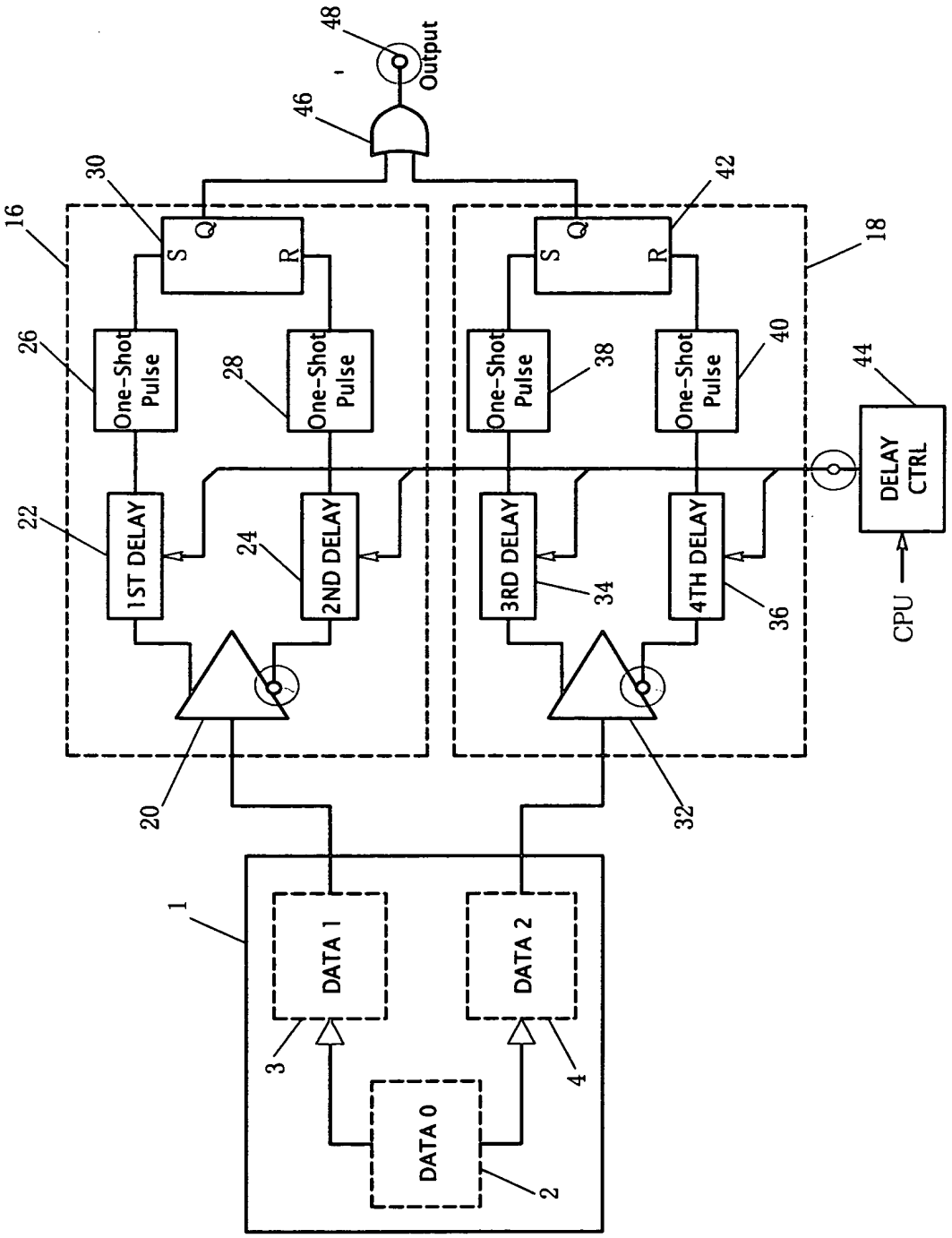
48
Output
46
30
42
16
18
S
Q
R
S
Q
R
26
One-Shot Pulse
28
One-Shot Pulse
One-Shot Pulse
38
One-Shot Pulse
40
44
DELAY CTRL
22
1ST DELAY
24
2ND DELAY
3RD DELAY
34
4TH DELAY
36
CPU
20
32
1
DATA 1
DATA 2
3
4
DATA 0
2

FIG. 11